Buried power rails and backside power distribution for nanometer-scale IC design

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Abstract. Buried power rails (BPR) and backside power delivery networks (BSPDN) technologies are promising tools for reducing the size of CMOS circuits. They provide significant improvements in many system-level parameters, such as IR-drop and power losses are reduced by more than 2 times, and by more than 4 times when using a buried power rail made of ruthenium, and the delay on critical paths and the overall area of the circuit are also significantly reduced. However, to fully realize the potential of this technology, a number of process and architectural issues need to be addressed. In this paper, the authors discuss the prospects and challenges associated with the implementation of buried power rails and backside power distribution networks. The physical characteristics of the semiconductor devices were also selected for process simulation in the Synopsys Sentaurus TCAD environment, as well as for physical synthesis in commercial CAD systems and open-source software. The developed models and methods will be included in the open flow for CMOS integrated circuits design with a 15 nm process and below.

1. Introduction

As a rule, a decrease in size in the technological nodes of semiconductor technologies is achieved by reducing the pitch of metal and contact polysilicon gate, but in modern CMOS technologies with dimensions about 10 nm and below the specific resistance of the metal increases significantly due to an increase in the effect of dimensional effects, including dispersion of the charge carriers on the surface and boundaries of grains [1.2]. Such an increase in specific resistance contributes to a greater voltage drop and becomes a significant obstacle to high-performance CMOS designs with technological dimensions of less than 5 nm. To ensure a lower voltage drop, developers often have to sacrifice compactness to create more reliable power delivery networks (PDN).

To solve this problem in a number of publications, the technology of buried power rails (BPR) was proposed as optimizing semiconductor CMOP devices with dimensions of less than 10 nm, which reduce the area of standard cells, voltage drop and power loss. In BPR technology, the power rails are located in silicon wafer and are excreted through special holes for connecting the power supply in

front or rear. A buried power rail with a high aspect ratio minimizes the drop in voltage and power due to the use of the channel with less resistance to supply to transistors [3]. It is also necessary to take into account the parasitic effects that occur on other components of the power supply (for example, on the printed circuit board, beam-lead package, the heterogeneities of metal conductors, etc.) and lead to a voltage drop in the occurrence of short-term current surges. The influence of these effects can be reduced by increasing the container of the interchange on the crystal. In BPR technology, routing is laid under a wafer where signals do not pass, and power rails with low resistance and a high aspect ratio increase the coupling capacitance between the power and ground, which reduces the voltage drop, associated with a peak current in the circuit.

To determine the possibilities of introducing BPR and BSPDN technologies in the traditional design flow for IC with dimensions of 15 nm and below, we have identified the main physical parameters of a technological model, physical synthesis and process simulation of CMOS ICs that are designed using these promising technologies.

2. Materials and methods

The traditional PDN is designed for the most efficient supply and reference voltage to active devices on the chip. Traditionally, it is implemented as a network of metal wires with low resistance made in the BEOL (Back-End-of-Line) on the front side of the wafer [4]. The power supply network shares this space with the signal interconnects. To supply power from the package to the transistors, electrons pass through all 15-20 BEOL layers via metal connections and windows, that become increasingly narrow, and therefore, more resistive, when approaching transistors. Along the way, they lose energy, which leads to a voltage and power drop. At the level of the standard cell, electrons are in VDD/VSS rails, from where they are connected to the source and drain of each transistor via an intermediate interconnect network (Figure 1).

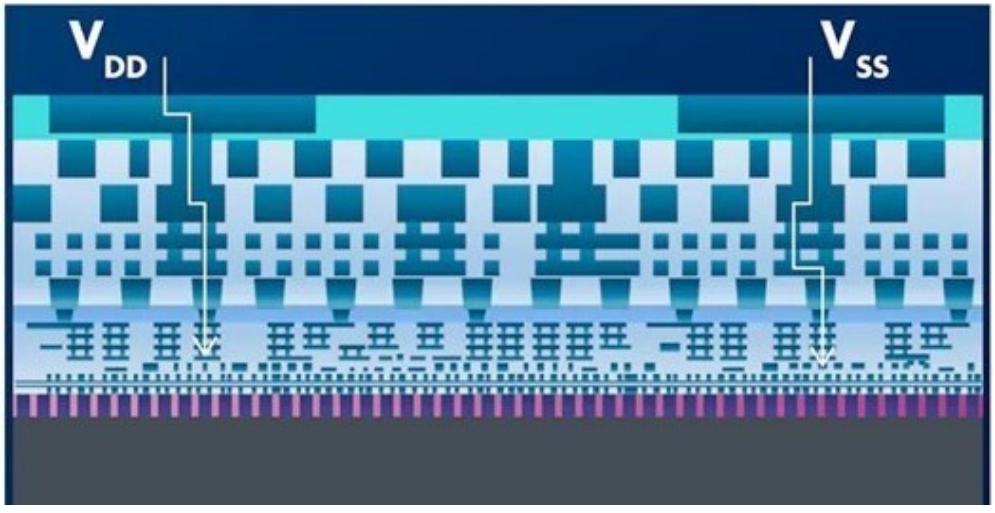

Figure 1. Traditional power delivery network

Traditional BEOL architecture designers face difficult challenges when scaling process sizes. Power/ground rails increasingly compete for resources in the design flow, accounting for at least 20 percent of routing resources. In addition, power/ground rails take up significantly more area at the standard cell level, limiting further increases in cell height. At the system level, power degradation and IR-drop impacts increase dramatically, forcing designers to increase voltage and power margins to ensure reliable signal transfer between external pins and transistors.

The idea behind BSPDN technology is to decouple the power delivery network from the rest of the routing by moving the entire power delivery network to the back side of the silicon wafer (Figure 2) [5, 6]. This allows power to be delivered directly to standard cells over wider, lower resistance metal lines, without the need for electrons to pass through a complex BEOL system. This approach reduces voltage and power losses, improves the performance of the power delivery network, reduces routing congestion in the BEOL, and allows for additional increases in standard cell height [7].

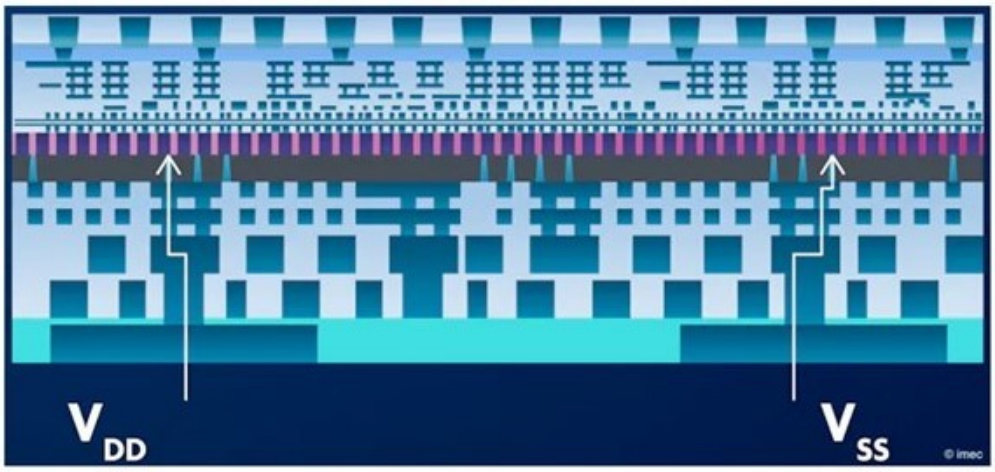

Figure 2. Backside PDN

There are three main approaches to forming a BSPDN (Figure 3) [8]:

1. The through-hole power rail TSV-middle is located near the active top layer and connects BSM1 (metal 1 on the back side) to the active top layer to supply power to the cells [9].

2. The buried power rail (BPR) is formed close to the active top layer (VBPR), the BPR layer plays the role of BSM1 (thus, in fact, one level of “reverse” power is moved to the front side) [10].

3. Contact with the back side when power is turned on is made through taps in the rail, BSM1 is aligned with the gate [11].

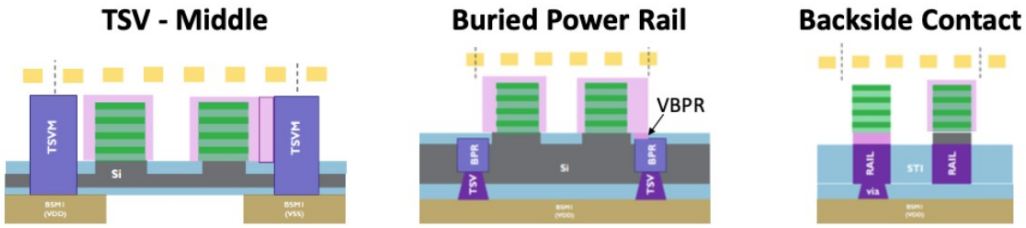

Figure 3. BSPDN variants

BPR technology further increases the standard cell height and reduces the IR-drop effect [12]. Instead of the standard BEOL implementation of power networks at the level of standard cells, in this technology the metal structure of the power networks is located under the transistors - partly in the silicon substrate, partly in the insulating oxide with fine grooves (Figure 4). This transfer of power supply networks from BEOL to FEOL [13] allows to reduce the number of metal tracks for supplying power to the transistors, which ensures a further reduction in the area of a standard cell (by 15-20%) [14]. In addition, when designing BRP perpendicular to a standard cell, it is possible to make narrow power rails, which reduces the peak current in the power networks.

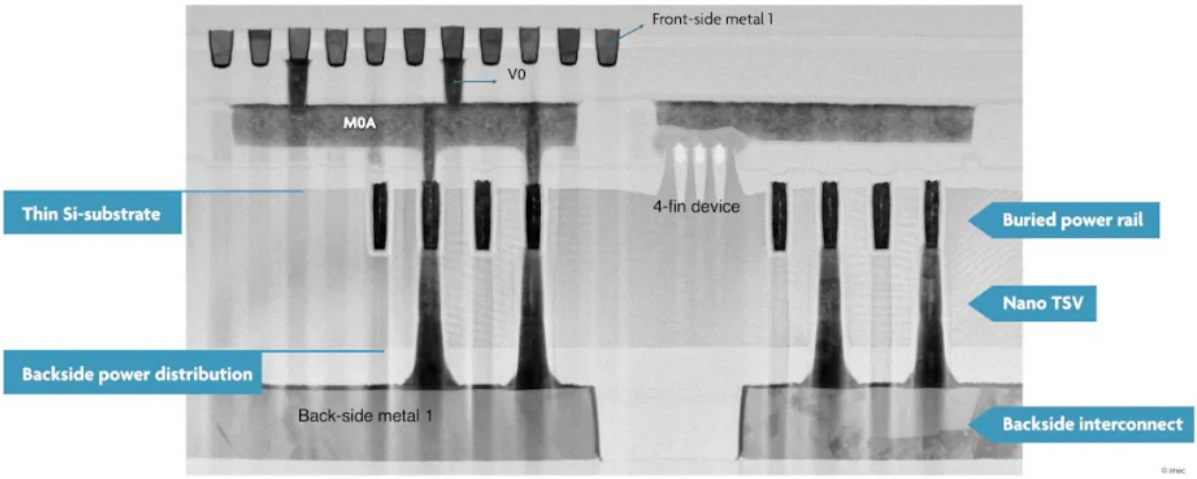

Figure 4. Sharing BPR and BSPDN technologies

According to preliminary calculations, the use of BSPDN and BPR will lead to a decrease in power consumption of up to 8% and a decrease in area of up to 24% for integrated circuits with 3 nm technology [15].

3. Results and discussion

Four different power supply configurations were considered:

1. FS – signal and power networks are routed to the top surface of the chip;
2. BS – signal and power networks are routed to the bottom surface of the chip;
3. FSBPR – signal networks are routed to the top surface of the chip, the power networks for standard cells are buried in the wafer;
4. BSBPR – signal networks are routed to the bottom surface of the chip; the power networks are buried.

The power rails in the FS BEOL configuration provide up to a 35% reduction in voltage drop [16]. When replaced with the FSBPR configuration, the voltage drop is reduced by an additional 27%. For the BSBPR configuration, the voltage drop is reduced by 85% [17]. In the conventional FS BEOL configuration, designers have to save routing resources to achieve the target values of the required voltage range (typically 10% of VDD), which can increase overhead and reduce processor performance. The BSBPR configuration completely eliminates the dependence between signal bandwidth and performance by completely isolating the signal networks from the power supply networks. For further research and process simulation, this configuration will be used.

Buried power rails implemented using ruthenium (Ru) or wolfram (W) can withstand high processing temperatures at the beginning of the process. In addition, Ru and W have lower resistivity than copper since the metal width is less than 20 nm [18]. The complete system is assembled by gluing the formed CMOS wafer (including metallization) to the carrier substrate. The CMOS substrate is then thinned to an extremely thin thickness (about 500 nm) for processing the metal on the back side. A through-hole nano-TSV connects the power network to the signal network for powering standard cells [19]. The following process steps result in an efficient power delivery system located on the back side of the substrate and partially inside it (Figure 5).

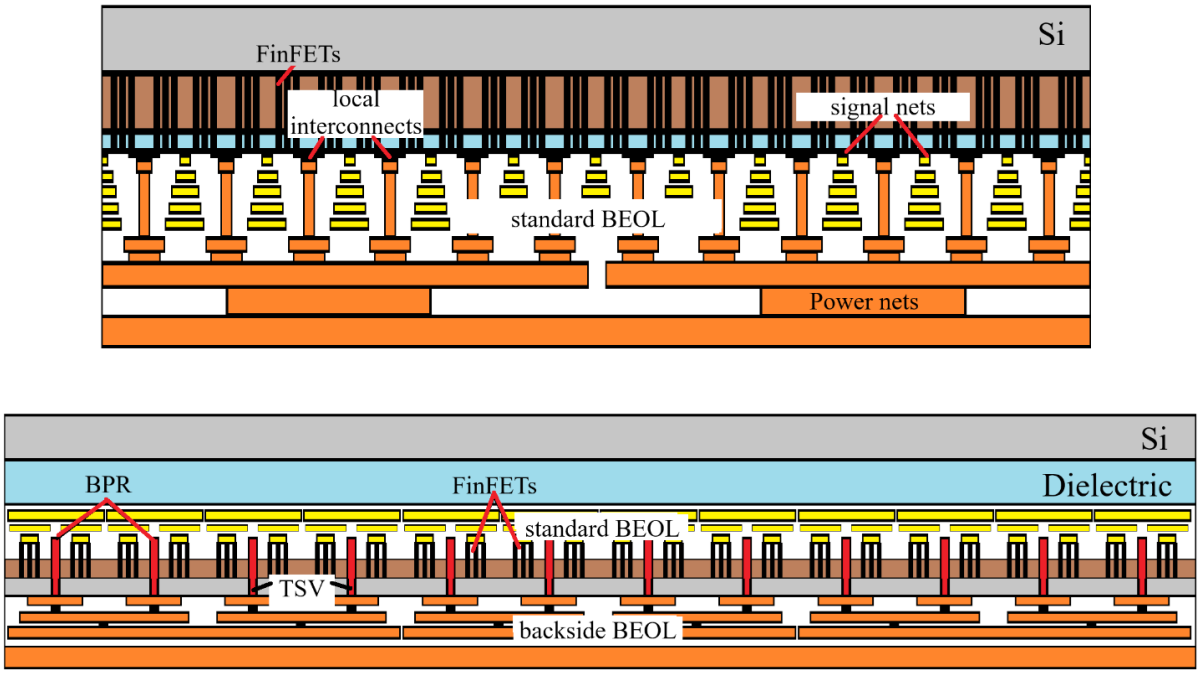

Figure 5. Differences in PDN

To perform physical synthesis of nanometer ICs with BSPDN and BPR technologies, open-source PDKs for 3-nm [20] and 15-nm technologies [21] with FinFETs will be used. The following physical parameters were selected to simulate the technological model (Table 1).

Table 1. Parameters of devices for BSPDN и BPR modeling

Layer	Parameter	Value
FEOL	Fin pitch	24 нм
	Fin width	6 нм
	Gate pitch	45 нм
	Gate width	16 нм
	STD cell height	120 нм
	Dielectric const	3.9
BEOL	Power pin width	36 нм
	M1 pitch	30 нм
	M0, M2, M3 pitch	24 нм
	M4-M11 pitch	64 нм
	M12, M13 pitch	720 нм
	BM1, BM2 pitch	720 нм
	Aspect Ratio	1.5
	Dielectric const	2.5

According to the results of studying publications, the values of technological parameters indicated in the table will give the best start for creating a model of nanometer semiconductor devices, as well as subsequent technological modeling and physical synthesis in commercial CAD systems, in open design flows, and also in educational software packages developed at the National Research University of Electronic Technology "MIET".

One of the main challenges associated with BSPDN technology is temperature control, since the heat sink is located above the carrier substrate [22]. In a BSPDN configuration, a dielectric connection between the active layers and the carrier substrate can be used. This connection layer increases the thermal resistance of the connection to the environment. Although the wide metal surface area promotes heat dissipation, the thin silicon wafer increases the thermal resistance compared to a thicker silicon substrate, which can lead to the formation of large hot spots [23]. Therefore, the issue of heat dissipation for systems with BSPDN technology remains open, and a solution to this issue will be sought in future work.

To place the power delivery network on the substrate from the back side, it is necessary to pass through the embedded rails, nano-TSV, metal interconnects of the signal input and output networks, which increases the parasitic capacitance of the interconnects by more than 2 times, and 90% of the parasitic capacitance falls on the embedded rails and nano-TSV. With further reduction in the technology size using these optimization methods, a multiple increase in parasitic capacitance is expected. This problem can be partially solved by isolating internal channels, but a complete solution has not yet been found.

At this stage of work in our laboratory, we are constructing a process model of CMOS structures with BSPDN technology to assess the prospects of its use in the physical synthesis flow, calculating the degradation of the main parameters of the circuit and overheating due to the increased influence of parasitic effects. Based on the results of the research, process modeling will be carried out, a set of measures will be proposed to reduce parasitic capacitances and stabilize the technological process to increase the yield.

4. Conclusion

This article provides a brief description of the advantages, disadvantages and prospects of backside power delivery networks and buried power rails. At the moment, the most advanced developments in the world are aimed at achieving the 2nm level, and BSPDN and BPR technologies look quite promising for solving this problem. And it will be possible to design and produce more efficient and compact nanometer integrated circuits due to a significant reduction in circuit size, voltage drop and power loss. Preliminary studies show significant advantages of their use, however, a number of issues related to the technological process and design reliability need to be resolved. The selected technological parameters and open PDKs will be used for technological modeling in commercial and open CAD systems to determine methods for mitigating the negative effects of BSPDN and BPR technologies without losing the advantages.

Acknowledgments

The study was conducted under the framework of the state assignment for the Federal project of the national project "Science and Universities" of the Ministry of Science and Higher Education of the Russian Federation for the National Research University of Electronic Technology - MIET, code 460 GZ-NIL PSS (FSMR-2024-0009), agreement No. 075-03-2024-061/3 dated 04/15/2024.

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